WHAT IS CLAIMED IS:

1. A process for forming an array of pixel cells comprising the steps of:

forming a sacrificial layer on top of an upper intermetal dielectric layer;

forming a photoresist mask over the sacrificial layer in a checkerboard pattern which includes a plurality of masked squares but which excludes corners of the masked squares;

etching unmasked portions of the sacrificial layer to stop on the upper intermetal dielectric layer, leaving a raised portion of the sacrificial layer having a top and sidewalls;

removing the photoresist mask;

forming a first dielectric layer over the upper intermetal dielectric layer and the top of the sacrificial layer, the first dielectric layer conforming to the sidewalls;

etching the first dielectric layer to remove the first dielectric layer over the upper intermetal dielectric layer while leaving vertical dielectric spacer structures along the sidewalls;

removing the raised portions of the sacrificial layer to leave the dielectric spacer structures.

forming a metal layer over the upper intermetal dielectric layer and the dielectric spacer structures; and

chemical-mechanical polishing the metal layer to form a substantially planar metal electrode surface including intervening dielectric structures.

2. The process according to claim 1 further comprising the steps of:

forming a second dielectric layer over the metal layer; and

chemical-mechanical polishing through the second dielectric layer into the metal layer to form the substantially planar metal electrode surface.

3. The process according to claim 1 further comprising the steps of:

forming a second dielectric layer over the metal layer, the second dielectric layer having a lower portion;

chemical-mechanical polishing through the metal layer to stop on the lower portion of the second dielectric layer; and

removing the lower portion of the second dielectric layer by wet etching.

4. The process according to claim 1 wherein the step of forming the photoresist mask comprises:

forming a photoresist layer in the checkerboard pattern which excludes corners of the masked squares; and

developing the photoresist layer.

5. The process according to claim 1 wherein the step of forming the photoresist mask comprises:

forming a photoresist mask in the checkerboard pattern; and

developing the photoresist layer such that corners of the masked squares are excluded.

6. The process according to claim 1 wherein the step of forming the photoresist mask comprises:

forming a photoresist layer in the checkerboard pattern which includes tabs connecting corners of diagonally-situated masked squares; and

developing the photoresist layer such that corners of the masked squares are excluded.

7. The process according to claim 1 wherein the step of forming the first and the second dielectric layers comprises forming a layer of silicon oxide.

8. The process according to claim 1 wherein the step of forming the first and the second dielectric layers comprises forming a layer of silicon nitride.

9. The process according to claim 1 wherein the step of forming the first dielectric layer comprises forming a layer of a low-k dielectric material selected from the group consisting of fluorosilicate glass, nanoporous silica, and organic polymers.

10. An apparatus including an array of pixel cells for a light valve formed by the process of claim 1.

11. An apparatus including an array of pixel cells for a light valve, the apparatus comprising:

an array of pixel cells arranged in a checkerboard pattern having a first set of squares alternating with a second set of squares, the first set of squares and the second set of squares formed from a first metal layer and lacking corners; and

dielectric spacer structures having a thickness intervening between the first set of squares and the second set of squares.

12. The apparatus according to claim 11 wherein the dielectric spacer structures are composed of silicon oxide.

13. The apparatus according to claim 11 wherein the dielectric spacer structures are composed of silicon nitride.

14. The apparatus according to claim 11 wherein the dielectric spacer structures are composed of a low-k dielectric material selected from the group consisting of fluorosilicate glass, nanoporous silica, and organic polymers.